AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A control unit for executing data communication between itself and another control unit, the control unit outputting a signal for resetting said another control unit through a bus line when the control unit is reset, comprising:

a CPU which is operated in accordance with a prescribed program;

a watchdog timer for monitoring operations of the CPU and outputting a reset signal to return the CPU to an initial condition when an abnormal state of the CPU is detected;

a high frequency oscillator for producing first clock pulses for operating the CPU at a first frequency;

a low frequency oscillator for producing second clock pulses for operating the CPU at a second frequency which is lower than said first frequency;

[[an]] exchanging means for exchanging clock pulses for operating the CPU from said first clock pulses to said second clock pulses when a prescribed condition is satisfied, thereby shifting the CPU to a low power consumed state;

abnormality detecting means for detecting abnormality of the low frequency oscillator; and

exchange stopping means for stopping exchange of the clock pulses by said exchanging means if [[the]] said abnormality detecting means detects the abnormality when said prescribed condition is satisfied.

Claim 2 (original): A control unit according claim 1, wherein said abnormality detecting means includes a counting means for counting the second clock pulses produced from said low frequency oscillator while said CPU is operated at the first frequency.

Claim 3 (Currently Amended): A control unit according to claim 1, wherein said exchange stopping means sends an exchange request signal to ~~other~~ the another control unit so that they are shifted into the low power consumed state even the CPU corresponding to said exchange stopping means cannot be shifted into the low power consumed state.

Claim 4 (Currently Amended): A control unit according to claim 2, wherein said exchange stopping means sends an exchange request signal to ~~other~~ the another control ~~units~~ unit so that they are shifted into the low power consumed state even when the CPU corresponding to said exchange stopping means cannot be shifted into the low power consumed state.

Claim 5 (Currently Amended): A multiplex communication system for executing data communications among control units which are interconnected via a bus line, one of the control units outputting a signal for resetting other control units via the bus line when the control unit is reset, wherein each said control units comprises:

a CPU which is operated in accordance with a prescribed program;

a watchdog timer for monitoring operations of the CPU and outputting a reset signal to return the CPU to an initial condition when an abnormal state of the CPU is detected;

a high frequency oscillator for producing first clock pulses for operating the CPU at a first frequency;

a low frequency oscillator for producing second clock pulses for operating the CPU at a second frequency which is lower than said first frequency;

[[an]] exchanging means for exchanging clock pulses for operating the CPU from said first clock pulses to said second clock pulses when a prescribed condition is satisfied, thereby shifting the CPU to a low power consumed state;

abnormality detecting means for detecting abnormality of the low frequency oscillator; and

exchange stopping means for stopping exchange of the clock pulses by said exchange means if [[the]] said abnormality detecting means detects the abnormality when said prescribed condition is satisfied.